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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/686,061	10/14/2003	Shailender Chaudhry	SUN04-0182	6999

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EXAMINER	
ZALEPA, GEORGE D	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 03/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/686,061	CHAUDHRY ET AL.	
	Examiner	Art Unit	
	George D. Zalepa	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,11-20 and 23-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9,10,21 and 22* is/are allowed.

6)☒ Claim(s) *1-8,11-20 and 23-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/19/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-25 have been examined.

Papers Submitted

2. The declaration as filed on 14 October 2003. Information Disclosure Statement as filed on 19 January 2006

Specification

3. The disclosure is objected to because of the following informalities: Paragraph 0025 refers to a "processor 100". This element number is not labeled within Fig. 1. Applicant is requested to appropriately make any changes to correct this error.

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Selectively deferring instructions issued in program order utilizing a checkpoint and multiple deferral scheme.

Claim Objections

4. Claim 3 states, "...executing other deferred instructions that *able to be* executed in program order." The following correction is suggested, "...executing other deferred instructions that **are** *able to be* executed in program order."

5. Claim 7 is objected to because of the following informalities: **Claim 7** states "The method of claim 1, wherein keeping track of data dependencies..." There is no reference to keeping track of data dependencies within **claim 1**. Applicant is suggested to make an appropriate change to clarify the scope of the claim.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-8 and 11-20, and 23-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Gupta et al (US Pat. No. 5,881,280).

8. Regarding **independent claim 1**,

9. Gupta discloses a method for deferring execution of instructions with unresolved data dependencies [see Gupta, Abstract, lines 5-8] as they are issued for execution in program order [see Gupta, Col. 5, lines 28-29], comprising: issuing instructions for execution in program order during a normal execution mode [see Gupta, Col. 5, lines 28-29]; and upon encountering an unresolved data dependency during execution of an instruction [see Gupta, Col. 2, line 4, lines 18-21], generating a checkpoint that can subsequently be used to return execution of the program to the point of the instruction [see Gupta, Col. 8, lines 34-41], deferring execution of the instruction [see Gupta, Col. 9, lines 59-61], and executing subsequent instructions in an execute-ahead mode, wherein instructions that cannot be executed because of an unresolved data dependency are deferred [see Gupta, Col. 8, lines 1-4], and wherein other non-deferred instructions are executed in program order [see Gupta, Col. 6, lines 5-8; Examiner's note: It would have been inherent that since only exceptions are deferred, that instructions completing without exceptions would have been executed normally, as was common in the art at the time of invention.].

10. Regarding **claim 2**,

11. Gupta discloses *the method of claim 1, wherein if the unresolved data dependency is resolved during execute-ahead mode, the method further comprises: executing deferred instructions in a deferred execution mode* [see Gupta, Col. 10, lines 37-39]*; and if all deferred instructions are executed, returning*

to the normal execution mode to resume normal program execution from the point where the execute-ahead mode left off [see Gupta, Col. 11, lines 29-42].

12. Regarding **claim 3**,

13. Gupta discloses *the method of claim 2, wherein executing deferred instructions in the deferred execution mode involves: issuing deferred instructions for execution in program order* [see Gupta, Col. 12, lines 39-41; lines 49-53]*; deferring execution of deferred instructions that still cannot be executed because of unresolved data dependencies* [see Gupta, Col. 10, lines 61-65; Col. 12, lines 44-48; Examiner's note: Gupta discloses upon checking a deferred exception executing those instructions that are in the speculative chain, thus deferring exceptions that are unresolved (not in the speculative chain)]*; and executing other deferred instructions that able to be executed in program order* [see Gupta, Col. 12, lines 49-53].

14. Regarding **claim 4**,

15. Gupta discloses *the method of claim 3, wherein if some deferred instruction are deferred again, the method further comprises returning to execute-ahead mode at the point where execute-ahead mode left off* [see Gupta, Fig. 6, elements 222 and 234; Col. 12, lines 53-55; Examiner's note: In these citations Gupta discloses a processor re-executing deferred instructions within a speculative chain until the point in the program where the fix up was initiated was reached, thus returning the processor to the state where the processor stopped to begin re-execution.].

16. Regarding **claim 5**,

17. Gupta discloses *the method of claim 2, wherein generating the checkpoint involves saving a precise architectural state of the processor to facilitate subsequent recovery from exceptions that arise during execute-ahead mode or deferred mode* [see Gupta, Col. 9, lines 9-13; Examiner's note: Gupta discloses the use of Pentium processors at the time of invention. At the time of invention, it would have been

inherent that a processor that utilizes speculation would utilize precise exception handling, such as the Pentium processors disclosed by Gupta at the time of invention.].

18. Regarding **claim 6**,

19. Gupta discloses *the method of claim 1, wherein executing instructions involves keeping track of data dependencies to facilitate determining if an instruction is subject to an unresolved data dependency* [see Gupta, Col. 9, lines 59-61].

20. Regarding **claim 7**,

21. Gupta discloses *the method of claim 1, wherein keeping track of data dependencies involves maintaining state information for each register* [see Gupta, Fig. 4, elements 84, 86, and 101], *which indicates whether or not a value in the register depends on an unresolved data-dependency* [see Gupta, Col. 9, lines 58-61].

22. Regarding **claim 8**,

23. Gupta discloses *the method of claim 1, wherein the unresolved data dependency can include: a use of an operand that has not returned from a preceding load miss; a use of an operand that has not returned from a preceding translation lookaside buffer (TLB) miss; a use of an operand that has not returned from a preceding full or partial read-after-write (RAW) from store buffer operation; and a use of an operand that depends on another operand that is subject to an unresolved data dependency* [see Gupta, Col. 2, lines 10-13; Examiner's note: Gupta does not explicitly disclose the situations when a data dependency could occur as the Applicant does in claim 8. However, it would have been inherent at the time of invention that the three given data dependency situations are common causes of speculative instruction exceptions. Furthermore, as previously mentioned, Gupta discloses the use of a caching system similar in spirit to the system within the Pentium series of processors. It would have been inherent that a modern processor at the time of invention isn't unlikely to include a translation lookaside buffer as disclosed by the Applicant.].

24. Regarding **claim 11**,

25. Gupta discloses *the method of claim 1, wherein deferring instructions involves storing instructions in a deferred buffer that is organized as a first-in first-out buffer* [see Gupta, Fig. 4, element 92; Col. 10, lines 61-65; Examiner's note: Although Gupta does not disclose a FIFO explicitly, it is clear from the disclosure that the re-execution register functions as a FIFO as it re-executes a chain of deferred exceptions beginning with the first exception generated in the chain.].

26. Regarding **claim 12**,

27. Gupta discloses *the method of claim 1, wherein issuing instructions for execution in program order involves issuing instructions from an instruction buffer that is organized as a first-in first-out buffer* [see Gupta, Col. 9, lines 10-13].

28. **Claims 13-20** and **23-25** are rejected as the apparatus performing the method of **claims 1-8** and **11-12** respectively.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George D. Zalepa whose telephone number is (571) 272-6754. The examiner can normally be reached on Monday-Friday (alt. Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GDZ

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